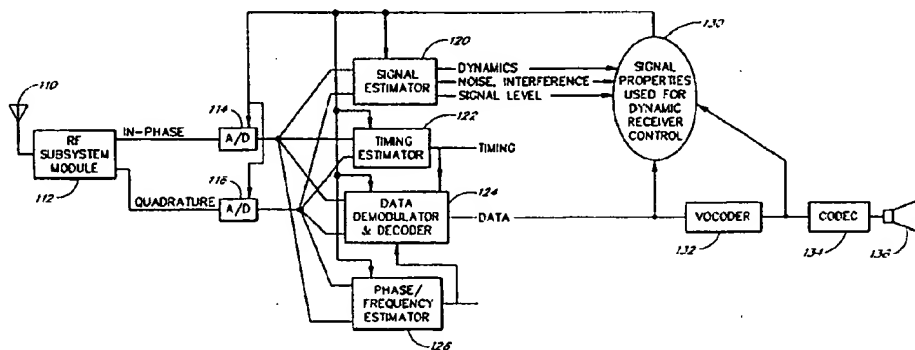




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(54) Title: ADAPTIVE WIRELESS COMMUNICATION RECEIVER



(57) Abstract

The present invention provides a method and apparatus for adaptive processing in a communication system receiver. The adaptive processing facilitates power savings and permits enhanced performance when necessary. This extends a receiver's operation time in receivers that operate on batteries, such as in cordless telephones or cellular telephones. A receiver adopting the principles of the present invention evaluates the characteristics and dynamics of an incoming signal, and based on the quality of the incoming signal, adjusts various aspects of the receiver such as the on-time correlators and analog to digital converters, the timing circuits, the despread equalizers, and the combiner. If the receiver comprises a receiver operation in accordance with GSM, the receiver may cycle the MLSE detection algorithms or cross correlation may be done over fewer data symbols.

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ADAPTIVE WIRELESS COMMUNICATION RECEIVERField of Invention

The present invention relates to the field of wireless communication and in particular to an adaptive receiver.

Background of the Invention

5 The field of wireless communications is rapidly expanding. In particular, cellular communication systems are experiencing phenomenal growth. Likewise, cordless telephones are in widespread use.

Each mobile station, whether a cordless or cellular telephone, operates using power supplied by an associated battery. Each mobile station continually draws power from the battery while in standby mode or during an active communication link. The mobile unit draws the most power during periods of an active communication link. In particular, 10 the receiver, which is responsible for obtaining, filtering, decoding and synthesizing the incoming signal, comprises a large percentage of total mobile unit power usage during an active communication link. This is especially true when the communication system comprises a modern cellular system, such as Global System for Mobile Communication (GSM) or a system adopting Code Division Multiple Access (CDMA) techniques. Modern communication systems adopt these complex coding schemes to increase both system capacity and voice quality.

15 Summary of the Invention

As known in the art, these complex coding and decoding schemes remain on or fixed during the duration of the communication link. Maintaining these complex coding and filtering schemes is desirable when the signal quality is poor, however, these schemes needlessly consume valuable power resources during periods of better or ideal channel quality. In addition, if the signal quality degrades below a tolerable threshold, these fixed receiver architectures result in dropped calls.

20 While advances in battery technology now provide more robust power sources, there still exists a need for a mobile station receiver having reduced power consumption. In addition, there is a need to provide more advanced processing in times of very low signal quality.

The present invention provides an adaptive wireless receiver which reduces power consumption in a receiver of a mobile station and/or increases performance. Reducing power consumption in a mobile station increases the duration of 25 time the mobile station may remain in standby mode or maintain an active communication link. Increasing performance provides better quality and fewer dropped calls.

In particular the system and method generally comprises dynamically adjusting receiver operation in response to signal quality.

30 One aspect of the present invention involves a power utilization control system for a wireless communication device. The system has a signal properties evaluation module operative to evaluate the characteristics of a received signal. The module is configured to provide an indication of the characteristics. At least one receiver component for the wireless communication device has at least two modes of operation and is responsive to the signal properties evaluation module to operate in at least one of the at least two modes of operation, based upon the characteristics. In one embodiment, the signal properties evaluation module is implemented using a digital signal processor. Preferably, the signal properties

evaluation module is configured to evaluate any signal dynamics such as signal noise levels or signal strength. In one embodiment, the wireless communications device operates in accordance with code division multiple access protocols.

In one embodiment, at least one receiver component is analog to digital converter configured to convert the received signal in an analog format to a received signal in a digital format. In this embodiment, the first mode involves operation at a first precision and the second mode involves operation at a second precision. In this embodiment, the power utilization control system further involves an analog to digital converter control module responsive to the signal properties evaluation module to select the precision of the at least one analog to digital converter based upon the indication of signal characteristics. Advantageously, the analog to digital converter control module is configured to select a lower bit precision for the at least one analog to digital converter when the signal is of generally high quality.

In another embodiment, the at least one receiver component comprises a timing estimator responsive to the indication of the characteristics from the signal properties evaluation module to alter timing estimation operation based upon the indication of signal characteristics. Advantageously, the timing estimator responds to the indication of the signal characteristics via a timing control unit to modify one or more of the timing estimator type, operation duty cycle, and bandwidth. The timing estimator may comprise a delay-lock-loop.

In one embodiment, the at least one receiver component comprises a plurality of despread modules responsive to the indication of the characteristics from the signal properties evaluation module to adjust operation based upon the indication of signal characteristics. Advantageously, the despread modules respond to the indication of the signal characteristics via a control unit to adapt one or more of the operation duty cycle or tap spacing in response to the indication of signal characteristics.

In yet another embodiment, at the least one receiver component comprises at least one equalizer responsive to the indication of signal characteristics from the signal properties evaluation module to change its operation based upon the indication of signal characteristics. Preferably, the equalizer alters one or more of its duty cycle or complexity of operation based upon the indication of signal quality.

In still another embodiment, the at least one receiver component comprises at least one correlator responsive to the indication of signal characteristics to operate in either the first or the second mode. Advantageously, the first mode comprises operation at a first precision and the second mode comprises operation at a second precision. The first mode of operation may further include a first duty cycle for the correlator and the second mode of operation comprises a second duty cycle for the at least one correlator.

In still another embodiment, the signal properties evaluation module provides the indication of characteristics via a control module. Thus, in one embodiment where the at least one receiver component comprises a plurality of correlators, the control module suspends operation of one or more of the plurality of correlators during periods when the signal is of relatively good quality.

In another embodiment, the at least one receiver component comprises a signal combiner responsive to the indication of signal characteristics from the signal properties evaluation module to alter operation of the combiner based upon the indication of signal characteristics. Advantageously, the at least two modes comprise at least first and second

modes, wherein in the first mode the combiner operates in accordance with a first processing algorithm and in the second mode, the signal combiner operates in accordance with a second processing algorithm. In one embodiment, the first algorithm comprises a more complex algorithm than the second algorithm.

5 In another embodiment, the at least one receiver component comprises a frequency estimation module, and wherein the at least two modes comprise at least first and second modes, selected in response to the indication of the signal characteristics from the signal properties evaluation module. Preferably, the at least two modes involve at least two algorithms having a difference in one or more of the processing precision, filter type, processing rate, or duty cycle. In a specific embodiment, the frequency estimation module responds to a demodulated pilot signal and to demodulated desired signals from users other than the intended receiver.

10 Another aspect of the present invention involves a method of reducing power consumption in a wireless communication receiver having a plurality of receiver components comprising receiving a signal, monitoring the characteristics of the incoming signal, evaluating the quality of the incoming signal based on the characteristics, and altering the operation of at least one of the receiver components based upon the evaluated quality of the incoming signal. Preferably, the at least one of the receiver components comprises an analog to digital converter. In one embodiment, 15 evaluating the quality of the incoming signal comprises determining the proper precision setting for the one or more analog to digital converters. For instance, altering the operation of the analog to digital converter may comprise altering the precision of the analog to digital converter. More specifically, altering the precision of the analog to digital converter comprises altering the precision between 5 bits and 2 or 3 bits, in the present embodiment.

20 In one embodiment, monitoring the characteristics of the incoming signal comprises monitoring any one or more of signal dynamics, signal noise, signal level, bit error rate, or frame error rate. In one embodiment, the method is implemented in a communication receiver operating in accordance with code division multiple access.

In another embodiment, the step of altering the operation of at least one of the receiver components comprises adjusting the operation of a signal timing estimator. Advantageously, the step of adjusting operation comprises reducing the duty cycle of the timing estimator and/or adjusting the filter properties of a timing estimator. In this embodiment, the step of monitoring the signal comprises monitoring any of signal dynamics, signal noise, and signal level. In a preferred 25 embodiment, the signal timing estimator comprises at least one delay lock loop.

In yet another embodiment, the step of altering the operation of at least one of the receiver components comprises altering the operation of an equalizer for an incoming signal, the method further comprising the steps of evaluating information regarding the characteristics of an incoming signal, and modifying the complexity of equalizer algorithms for the equalizer based upon the evaluation. 30

In another embodiment, the step of altering the operation of at least one of the receiver components comprises altering the operation of at least one correlator based upon the evaluation of the incoming signal. The step of altering the operation of at least one correlator advantageously comprises modifying the symbol frequency of operation of the correlator.

In yet another embodiment, the step of altering the operation of at least one of the receiver components comprises altering the operation of a signal combiner in response to the step of evaluating the quality of the incoming signal. Preferably, the step of altering the operation of a signal combiner comprises selecting one of at least two algorithms operable with the combiner.

5 In still another embodiment, the step of altering the operation of at least one of the receiver components comprises altering the operation of a frequency estimator in response to the step of evaluating the quality of the incoming signal. Advantageously, the step of altering the operation of a frequency estimator comprises selecting an algorithm from at least two algorithms operable for the frequency estimator. Either in combination, or separately, the step of altering the operation of the frequency estimator comprises selecting a precision for the frequency estimator and controlling active
10 periods for the frequency estimator.

Yet another aspect of the present invention involves an adaptive signal synchronization apparatus for a wireless receiver. The apparatus has a timing estimator, a signal properties evaluation module responsive to signal characteristics to evaluate an incoming signal, and a timing control module responsive to the signal properties evaluation module to control the operation of the timing estimator.

15 In one embodiment, the timing estimator includes at least one delay lock loop. Advantageously, the timing control unit is configured to adapt the percentage of time that the timing estimator operates and/or tap spacing of the timing estimator.

In one embodiment, the timing estimator, the signal properties evaluation module and the timing control module are operative in digital signal processor.

20 In one embodiment, the adaptive signal synchronization further has a plurality of despread modules responsive to an indication of signal characteristics from the signal properties evaluation module to adjust operation of despread modules.

Yet another aspect of the present invention involves an adaptive equalizer system for a wireless receiver comprising an equalizer operable in at least two modes to perform equalization on an incoming signal, a signal properties evaluation module responsive to signal characteristics to evaluate an incoming signal, and an equalizer controller responsive
25 to the signal properties evaluation module to select between the at least first and second modes.

In one embodiment, one or more of the equalizer controller and the signal properties evaluation module is embodied in a digital signal processor. In one embodiment, the signal properties evaluation module receives a plurality of characteristics of an incoming signal and responds to such characteristics to develop equalizer operating parameters. In one embodiment, the at least first and second modes of operation comprise a first mode in which the equalizer operates in
30 accordance with a first algorithm and a second mode wherein the equalizer operates in accordance with a second algorithm which is different from the first algorithm. In one embodiment, the receiver comprises a wireless communication receiver in a wireless communication system. Advantageously, the equalizer is configured to compensate for time delays introduced in a signal transmitted over a wireless medium.

Yet another aspect of the present invention involves a method for adaptive operation of an equalizer in a receiver
35 comprising receiving, equalizing and demodulating an incoming signal, evaluating the quality of the incoming signal, and

adapting the operation of an equalizer based on the step of evaluating. In one embodiment, the step of adapting the operation of an equalizer comprises shutting off the equalizer when the evaluating indicates the signal is of generally high quality. In one embodiment, the step of adapting the operation of an equalizer comprises reducing the computational complexity of the equalizer when the evaluating indicates the incoming signal is of generally high quality. Advantageously, the step of evaluating comprises evaluating any of signal dynamics, signal noise, signal level, bit error rate, or field error rate. In one embodiment, the step of evaluating comprises determining the rate of change of the signal characteristics over time.

Still another aspect of the present invention involves an adaptive combiner for a receiver comprising at least two correlators configured to receive an incoming signal, a combiner coupled to the at least two correlators, a signal properties evaluation module responsive to characteristics of a received signal to provide an indication of the properties of an incoming signal, and a combiner control module coupled to the combiner and responsive to the indication of signal characteristics from the signal properties evaluation module to alter operation of the combiner based upon the indication of the signal characteristics. In one embodiment, the combiner control module is further coupled to at least one of the at least two combiners, the combiner control module configured to provide a control signal to at least one of the at least two combiners to alter the operation of at least one of the at least two combiners. In one embodiment, at least one of the correlator, the combiner, the signal properties evaluation module and the combiner control module is embodied using a digital signal processor. In one embodiment, the combiner comprises part of a wireless communication receiver.

Yet another aspect of the present invention involves a method of adaptive control in a receiver comprising receiving an incoming radio signal, correlating at least portions of the incoming signal, combining the portions of the incoming signal, evaluating the quality of the incoming signal, and controlling the combining step based on the quality of the incoming signal. In one embodiment, the step of combining may proceed in accordance with a first or a second mode of operation, the first and second mode operating in accordance with different algorithms for the combining step, the controlling comprising changing the mode. Advantageously, the algorithms differ in the manner of parameter estimation used in the step of combining. In one embodiment, the step of evaluating comprises evaluating one or more of the signal dynamics, signal noise, signal level, bit error ratio, and frame error ratio.

Yet another aspect of the present invention involves a method for reducing power consumption in a receiver operating in accordance with any TDMA System, such as Global System for Mobile Communications comprising receiving a radio signal, evaluating signal dynamics of the radio signal, and altering a range of delays in a correlator based on the signal dynamics. In one embodiment, the step of evaluating comprises monitoring in a timing unit the rate of signal timing change over time. In one embodiment, the step of altering a range of delays comprises reducing the range of delays when the signal is determined to be generally stable based on the signal dynamics. Preferably, generally stable comprises a low rate of change over time or a signal wherein the signal does not demonstrate rapid timing drift from burst center. In a particular embodiment, reducing the range of delays comprises performing cross-correlation every ± 2 data symbols. In one embodiment, the step of evaluating comprises monitoring the center of a burst from burst to burst in the received radio

signal. In one embodiment, the step of altering a range of delays comprises increasing the range of delays and the signal dynamics indicate that the radio signal is generally unstable based on high signal dynamics.

5 Still a further aspect of the present invention involves an adaptive correlator for a communications receiver configured to receive an incoming signal comprising a correlation unit configured to compare the incoming signal to a known timing sequence, a timing recovery unit connected to the correlation unit, the timing recovery unit configured to evaluate the timing of the incoming signal, and a correlator controller connected to both of the timing recovery unit and the correlation unit, the correlation controller configured to adapt the operation of the correlation unit based on the evaluation by the timing recovery unit. In one embodiment, correlator controller is configured to adapt the operation of the correlation unit to reduce the number of symbols over which the correlation unit operates. Advantageously, the timing recovery unit is configured to determine the change in timing of the incoming signal over time, and the correlator unit is configured to perform a cross-correlation between the received signal and a known training sequence. In one embodiment, the communications receiver operates in accordance with the principles of a Global System For Mobile Communications.

15 Yet another aspect of the present invention involves a method of adaptive control in a receiver utilizing MLSE algorithms comprising receiving a signal, monitoring the level of the signal, monitoring the response of the incoming signal to a filter, and suspending operation of the MLSE algorithms when the signal level is high and the response to the filter indicates a generally clear channel. In one embodiment, a high signal level comprises a signal having level generally near the maximum signal level. Advantageously, monitoring the level comprises monitoring the output of a signal level estimator, and monitoring the response comprises monitoring the response of the incoming signal to a matched filter. In one embodiment, a generally clear channel comprises a response to the filter generally resembling an impulse. Preferably, suspending the MLSE algorithm comprises replacing the MLSE algorithm with a MSK demodulator. In one embodiment, the MSK demodulator comprises a bit-by-bit MSK demodulator.

20 Another aspect of the present invention involves an adaptive MLSE detector comprising a signal level estimator responsive to an incoming signal to determine the signal level of the incoming signal, a filter configured to filter the incoming signal, a MLSE detector configured to obtain input from the filter, the MLSE detector configured to compute signal probability, and a MLSE controller coupled to the signal level estimator, the filter and the MLSE detector, the MLSE controller configured to evaluate output from the signal level estimator and the filter and, based on the evaluation, control the operation of the MLSE detector. Advantageously, the filter comprises a matched filter and the MLSE controller is configured to suspend operation of the MLSE algorithms when the signal level estimator indicates the signal is generally high and the response to the signal is generally an impulse. In one embodiment, the MLSE controller is configured such that when the MLSE algorithms are suspended, the MSK demodulation occurs. Preferably, control of the operation involves reducing the power consumption.

Brief Description of the Drawings

Figure 1 is a block diagram of wireless communication system receiver.

35 Figure 2 illustrates the front end of a digital communication receiver with analog to digital converters incorporating signal quality feedback.

Figure 3 illustrates a timing estimator incorporating signal quality feedback.

Figure 4 illustrates equalizer incorporating signal properties feedback.

Figure 5 illustrates a basic block diagram of a combiner having adaptive performance.

Figure 6 illustrates a block diagram of a wireless communication receiver in a Global System for Mobile

5 Communications.

Figure 7 illustrates a frequency estimation block diagram for an adaptive frequency estimator.

Detailed Description of the Preferred Embodiments

Figure 1 illustrates the basic components of a wireless communication system receiver as embodied in a cellular telephone communication receiver adopting code division multiple access (CDMA). Modern cellular communication systems
10 generally comprise a plurality of base stations and mobile stations. Both of the base station and a mobile station incorporate a communication receiver. The present invention focuses on a system and method of reducing power consumption of a battery powered mobile station communication receiver and also, improving performance when necessary. The base stations are typically wired to a land based power source. For purposes of explanation, a general overview of a receiver in one preferred embodiment is provided below. In general, the receiver comprises an antenna 110
15 coupled to a radio frequency (RF) subsystems module 112. This module 112, provides two outputs (I,Q) to analog-to-digital (A/D) converters 114, 116. Each of the A/D converters 114, 116 connects to signal estimator 120, a timing estimator 122, a data demodulator 124, and a phase and frequency estimator 126. In turn, the output of the timing estimator 122 and the phase and frequency estimator 126 couple to inputs of the data demodulator 124. The output of the data demodulator 124 couples to a vocoder 132 and a signal properties evaluation module 130. The vocoder's output couples
20 to a codec 134 and the signal properties evaluation module 130. The output of the codec 134 couples to an amplified speaker 136 for audio reproduction.

In operation the antenna 110 converts arriving radio frequency signals to electrical signals for the radio frequency (RF) subsystems module 112. The RF subsystems module 112 amplifies the incoming signal before performing frequency translation and band pass filtering on the signal. The RF subsystem provides the in-phase (I) and quadrature-
25 phase (Q) portions of the incoming signal to A/D converters 114, 116. The A/D converters 114, 116 convert the incoming analog signal to a digital format. Conventionally, the A/D converters 114, 116 are configured with a predetermined precision for the conversion process.

The signals exiting the A/D converters 114, 116 enter the signal estimator 120, a timing estimator 122, a phase and frequency estimator 126, and a data demodulator 124. The output of the timing estimator 122, and phase and
30 frequency estimator 126 connect to the data demodulator 124 to provide data necessary for the demodulation and decoding of the voice signal.

The timing estimator 122 determines the timing of the signal in relation to a synchronization signal to obtain signal alignment during decoding and demodulation. In one preferred embodiment, the timing estimator 122 comprises a delay lock loop (DLL), which is described in more detail below in conjunction with Figure 3.

The phase and frequency estimator 126 determines the phase and frequency of the incoming signal which, as known by those familiar with receiver operation, aids in the demodulation process.

The signal estimator 120 determines the signal to noise ratio, signal dynamics, and the signal strength level and provides these values to the signal properties evaluation module 130. As discussed in more detail below, the signal properties evaluation module 130 uses these values for dynamic receiver control.

The data demodulator and decoder 124 demodulates the signal from radio frequency and performs reverse coding on the signal. In one embodiment the coding comprises code division multiple access (CDMA).

The output of the data demodulator and decoder 124 is coupled to the signal properties evaluation module 130 and the vocoder 132. The signal properties evaluation module 130 uses the demodulated and decoded data to estimate the bit error rate (BER) and the frame error rate (FER) which in turn are used to further evaluate the incoming signal. The vocoder 132 generally comprises an electronic speech analyzer as known in the art.

The output of the vocoder 132 is coupled to a codec 134 input. As known in the art, the codec 134 converts the digital signal to an analog signal. The corresponding signal exits the codec 134 for receipt by a speaker 136 which audibly reproduces the signal. An optional amplifier, not shown, may exist between the codec 134 and the speaker 136.

Optionally, the signal may comprise data information which would not require conversion of the signal to an analog format. Hence, a receiver configured to process non-voice data would lack componentry for processing voice, such as the vocoder 132 and codec 134.

The signal properties evaluation module 130 provide feedback to the A/D converters 114, 116, the signal estimator 120, the timing estimator 122, the data demodulator and decoder 124, and the phase and frequency estimator 126 in accordance with various aspects of the present invention in order to facilitate dynamic control of the various blocks of the receiver for changing signal quality and/or power reduction purposes.

Analog to Digital Converters Incorporating Signal Quality Feedback

Figure 2 illustrates one embodiment of the present invention. At the front end of a receiver adopting CDMA principles, the signal is divided into its in-phase (I) and quadrature-phase (Q) components. Each of these respective signals enters one of the analog to digital converters 114, 116. The analog to digital converters 114, 116 converts the incoming analog signal to a digital representation of the signals.

In conventional systems, the precision of each A/D converter 114, 116 is held constant, typically at 5 bits. The output of the A/D converters 114, 116 couple to the other receiver subsystems 200. The receiver subsystems 200 comprises componentry such as the signal estimator 120, timing estimator 122, data demodulator 124, and the phase and frequency estimator 126, shown in greater detail in Figure 1. Accordingly, the precision of the A/D converters impacts the processing of the majority of the remaining receiver subsystems, as depicted in Figure 1. As explained previously in conjunction with Figure 1, the output of the signal estimator 120 connects to the signal properties evaluation module 130. The signal properties evaluation module 130 is in communication with the A/D converters via an A/D converter control module 220. The control decision module connects to each of the A/D converters 114, 116. Of course, the A/D converter control module 220 can be considered part of what could be combined with the signal properties evaluation module 130.

In other words, the control for the A/D converters 114, 116 can be generated directly from the signal properties evaluation module whereby the separate A/D converter control module 220, which receives input from the signal properties evaluation module 130, is made up of one module or multiple modules or combined with the signal properties evaluation module 130. The independent depiction in the figures of the present application is provided to facilitate the description of the system.

5 In operation, real-time feedback from the signal properties evaluation module 130 controls the operating precision of the A/D converters 114,116. In particular, the in-phase and quadrature phase components of the incoming signal enter the A/D converters 114,116. At the inception of the communication link, the precision of the A/D converters 114,116 is set to a first precision level, in one embodiment, the highest precision level provided by the A/D converters 114, 116. The A/D converters 114, 116 modify the incoming signal to a digital format and forward the signal to the other components of
10 the receiver. One component of the receiver which obtains the output of the A/D converters 114,116 is the signal estimator 120, which is incorporated in Figure 2 in the receiver subsystem 200. The signal estimator 120 evaluates the digitized signal to determine dynamics, noise and interferences level and the signal strength. These values are forwarded to signal properties evaluation module 130.

The evaluation module 130 processes the information from the signal estimator 120 (and other inputs as
15 depicted in Figure 1) and arrives at a determination of the signal quality and stability, referred to herein as the signal properties or characteristics. The signal properties are forwarded to the A/D converter control module 220 which evaluates the signal properties. Based on the evaluation of the incoming signal, the control module 220, which is in communication with the A/D converters 114,116, adjusts the precision level of the A/D converters. Advantageously, the A/D converters can be adjusted separately. An evaluation by the signal properties evaluation module 130 and the control
20 module 220 indicating a generally stable signal prompts the control module to reduce the precision of each of the A/D converters 114,116. If signal quality is high enough on I or Q, one or the other signals may be entirely shut off. In one embodiment, when the signal is of high quality the control module 220 reduces the precision of each or one of A/D converter 114,116 to four, three, or even two bits. Reducing the precision of the A/D converters 114,116 reduces the power consumption of the receiver. Because the control module 220 only reduces the precision of the A/D converters
25 114,116 when the incoming signal is of high quality, the power consumption of the mobile station decreases without a compromise in audio quality. Because the precision of the A/D converters can drastically increase or decrease the total amount of data which must be processed by the remaining receiver components such as the signal estimator 120, the timing estimator 122, the data demodulator and decoder 124, and the phase and frequency estimator 126, the power savings resulting from the reduction of precision in the A/D converters 114, 116 can significantly impact the power
30 consumption of the receiver. As further shown in Figure 2, the control module 220 also connects to the receiver subsystems 200 to appropriately adjust the operating precision of the other aspects of the receiver. In particular, when the control module 220 reduces the precision (number of bits) of the A/D converters 114,116, the components which receive the output of the A/D converters will also operate in a reduced precision mode. If one of the I or Q signals is completely discontinued due to very high signal quality on the other signal, receiver subsystems which respond to the
35 particular signal which has been discontinued would be completely deactivated in one embodiment, further reducing power.

Conversely, if the evaluation module 130 and control module 220 ascertain that the signal quality is poor, the control module increases the precision of either or both of the A/D converters 114, 116. In this fashion the precision of the A/D converters 114, 116 dynamically adjust depending on the quality of the incoming signal.

The degree or percentage of power consumption achieved using these principles varies depending on the receiver subsystems 200 components. In one embodiment, the reduction in operating precision in the front end A/D converters 114, 116 can result in an overall reduction in receiver power consumption of about 20 percent, while degrading signal quality by less than about .8 Db. This correlates to an overall reduction in chip power usage of approximately 5% to 10% in the present embodiment. Furthermore, with the reduction in power consumption during periods of high signal quality, for the same power usage over time, the precision of the A/D converters 114, 116 can be increased during periods of poor signal quality to enhance communication performance without increasing the overall power usage over time.

Timing Estimator Incorporating Signal Quality Feedback

Modern communication receivers utilize some form of signal synchronization to properly track, demodulate and decode the incoming signal. One example of such a synchronization mechanism is a delay lock loop which serves to synchronize the incoming signal with an internal or known clock or timing signal. Figure 3 illustrates a synchronization mechanism known as a timing estimator incorporating signal quality feedback.

A receiver includes a number of despreaders 300, each coupled to a timing estimator and filter module 122 (e.g., a delay lock-loop or DLL). The output of the timing estimator and filter module 122 connects to the data demodulator, as shown in Figure 1. Also shown in Figure 3 is the signal properties evaluation module 130 which obtains information regarding the incoming signal and, upon processing the information, determines the quality and/or dynamics of the incoming signal. The output of the signal properties evaluation module 130 connects to a timing control decision unit 320. The output of the signal properties evaluation module couples to each of the despreaders 300 and the timing estimator and filter module 122 via the timing control decision unit 320.

In conventional systems, the timing estimator and filter module 122, (e.g., the DLL), operates constantly, and at a fixed rate of sampling. However, in accordance with the principles of the present invention, the timing estimator and filter module 122 can operate all the time, intermittently, or at a reduced rate.

In the present embodiment, each of the despreaders 300 outputs a signal recovered from the spread spectrum data transmission to the timing estimator and filter module 122. The timing estimator and filter module 122 receives and processes the despread signals to synchronize the signals. A timing signal is provided to the demodulation unit 124 (Figure 1) for use in demodulation.

The signal properties evaluation module 130 simultaneously provides information regarding the quality and/or dynamics of the incoming signal to the timing control decision unit 320. The timing control decision unit 320 evaluates the information describing the incoming signal properties and provides control information to the timing estimator and filter module 122 and each of the despreaders 300.

The timing estimator and filter module 122 and each of the despreaders 300 may alter its operation based on the input from the timing control decision module 320. For example, the timing control decision module 320 provides data to

the timing estimator and filter 122 to thereby control the type, operation duty cycle, and filter properties, such as complexity and bandwidth. The information provided from the timing control decision unit 320 to the timing estimator 122 changes depending on the quality of the signal. The timing estimator and filter module 122 uses this information to adjust its operation to save power when the incoming signal is of high quality and/or increase performance during periods of low signal quality and/or high dynamics.

More specifically, based on the timing error, the DLL 122 can modify its operation. For instance, if the timing error becomes very small on repetitive samples, the duty cycle, or percentage of time that the DLL 122 operates, can be adapted to save power. In other words, in periods of small error in timing, the duty cycle of the DLL 122 can be decreased for less frequent operation. In times of higher timing error, the duty cycle of the DLL 122 can be advanced for more frequent sampling. Similarly, the DLL type can be adjusted for better or poorer timing error. Furthermore, the DLL type can be altered during periods such as pull-in or reacquisition to provide necessary performance during these periods. For example, during pull-in, the DLL may utilize four taps and then adjust the tap spacing to two when the delay is estimated. Accordingly, only the processing complexity necessary to maintain signal timing is required.

As known in the art, timing estimators and associated filters, such as a DLL, begin operation after the initial signal search process occurs to achieve precise synchronization and tracking. The DLL generally comprises a first correlator beginning operation early and a second correlator beginning operation later in relation to the optimum sampling time. An error signal is formed by taking the difference between the two absolute values of the two correlator outputs. A non-zero error signal indicates that the timing of the synchronizing signal is incorrect relative to the optimum sampling time. Accordingly, the synchronization signal is either retarded or advanced, depending on the sign of the error. Operating this loop adjusts the synchronization signal.

During periods of general stability with regard to the incoming signal, the error signal is generally zero and hence the timing of the synchronization signal remains generally unchanged. Alternatively, when the incoming signal is generally unstable and possesses high dynamics or interference, the error signal is generally non-zero and the timing estimator 122 continually evaluates and adjusts the synchronization signal.

Based on the above described operation of an embodiment of the present invention using a DLL, the timing control decision unit 320 evaluates the incoming signal based on input from the signal properties evaluation unit 130 and adjusts the behavior of the DLL to use power efficiently and/or provide increased reliability in times of low signal quality. For example, during periods of general stability, the timing control decision unit 320 adjusts operation of the DLL by reducing the duty cycle, the complexity and/or bandwidth of the filters, all of which reduce power consumption of the receiver.

The timing control decision unit 320 also provides data to the despreaders 300 to control the tap spacing of the despreaders. The information provided from the timing control decision unit 320 to the despreaders 300 alters the operation of the despreaders to use power efficiently by reducing power usage during periods when the incoming signal is of superior quality. For example, the control information provided to the despreaders 300 may alter the despreaders tap spacing to save power during periods when the incoming signal is of high quality.

In this fashion the receiver monitors the quality of the incoming signal and adjusts the operation of the timing estimator and filter module 122 and the despreaders 300 to reduce the power consumption when the signal is of high quality and generally stable. Alternatively, during periods of poor signal quality, the operation is made more robust, at the cost of additional power consumption.

5 Equalizer Incorporating Signal Properties Feedback

Many modern communication systems, such as systems employing time division multiple access (TDMA) and code division multiple access (CDMA), often employ a type of receiver known as a RAKE receiver. A RAKE receiver has a number of receivers, or "fingers," each of which are configured to obtain a portion of a radio signal. Receivers employ such a configuration because, in most communication systems, the channel characteristics are unknown or time-variant. One example is when a transmitted signal encounters obstacles in the path between the transmitter and receiver. Because of the obstacles, the resulting signal includes energy peaks which are spread over time. In particular, the incoming signal is often separated into a number of peaks or time-varied portions each of which contain important signal information. Each of the fingers of a RAKE receiver obtains the information at each of the peaks of the incoming signal. However, the energy at each of the peaks may become misaligned or smeared, thereby preventing the fingers of the rake receiver from properly obtaining the signal.

To overcome the misalignment of the peaks in the incoming multipath signal, modern communication systems often employ equalizers. The equalizer removes certain time delayed waves or signal portions. In particular, equalizers detect the delayed portions of the signal and lock onto the strongest portions. Equalizers may operate by using a training sequence that is sent at the start of the data communications burst. The equalizer then adjusts itself to provide the maximum response on the channel, thereby negating the deteriorating effects of the radio channel itself.

Undesirably, the one or more equalizers in a receiver of a modern communication system operate continuously during an active communication link. The continuous operation of the equalizer is desirable when the peaks of a multipath signal are misaligned. However, continuous operation of the equalizers in a mobile station when the incoming signal is generally stable and not in need of equalization consumes valuable battery power. One embodiment of the present invention comprises adjusting the complexity and/or duty cycle of the equalizer based on the characteristics of the incoming signal to reduce power consumption and/or increase performance as needed.

Figure 4 illustrates one embodiment of an equalizer configured for adaptive operation in accordance with the principles of the present invention. In particular, with regard to signal equalization, the relevant portion of a wireless communication receiver comprises an equalizer 100 having a first input configured to receive a signal, a second input coupled to an output of an equalizer controller 410, and an output coupled to the demodulator 124. The input of the equalizer controller 410 couples to the output of the signal properties evaluation module 130, which is described above in greater detail.

In operation, the components illustrated in Figure 4 cooperate to receive a signal at the first input of the equalizer 400. In one embodiment, at start-up, the equalizer 400 enters a full operation mode wherein the signal improving capabilities of the equalizer are fully operational. After fully equalizing the incoming signal, the equalizer passes the signal

to the demodulator 124 for additional signal processing. The output of the demodulator 124 passes to other receiver subsystems (see Figure 1).

Other subsystems of the receiver (Figure 1) provide information regarding the signal to the signal properties evaluation module 130. The signal properties evaluation module 130 processes and feeds the processed information to the equalizer controller 410. The equalizer controller 410 further evaluates the signal characteristics based on the information from the signal properties evaluation module 130 and, based on this evaluation, outputs control information to the equalizer 400. The control information dictates the duty cycle and complexity of operation of the equalizer 400.

The amount of power used by the equalizer 400 depends upon the duty cycle of the equalizer 400 and the complexity of the equalizing algorithms used in the equalizer 400. In one embodiment, the equalizer 400 can be completely disabled when the peaks in an incoming signal are readily discernible and the equalizer can be re-activated when the peaks become "smeared." For example, the equalizer 400 enters a power saving mode when the signal properties evaluation module 130 and the equalizer controller 410 determine that the incoming signal no longer requires extensive equalization. Conversely, the equalizer returns to full equalization when instructed that the incoming signal requires equalization to maintain communication quality and prevent dropped calls. In this manner the equalizer's overall power consumption is minimized without sacrificing signal quality and communication link integrity.

RAKE Finger Duty Cycle Adjustment and Combiner Algorithms Adjustment

Figure 5 illustrates a combiner in a RAKE receiver. A CDMA receiver employs multiple correlators also known as fingers. The multiple correlators reduce a receiver's susceptibility to multipath components because the receiver can simultaneously receive several multipath signals and coherently combine them, resulting in a stronger signal. The RAKE receiver also enables a mobile station to communicate with two base stations simultaneously, making soft hand-offs possible and greatly reducing the probability of dropped calls.

Present systems operate every finger of the RAKE receiver at full precision during the entirety of each active communication link. Operating each finger of the RAKE receiver at full precision maintains audio quality during signal fading and when the signal contains multipath components. However, operating every finger of the RAKE receiver and the combiner at full precision when the incoming signal is of high quality needlessly consumes battery power. The embodiment described herein dynamically adjusts the duty cycle of the fingers of the RAKE receiver and varies the complexity of the combiner algorithms to save power when the signal is of high quality.

As shown in Figure 5, one preferred embodiment comprises several correlators 510, each of which couple to a combiner 516. The output of a combiner control module 550 couples to the combiner 516 and each of the correlators 510. The combiner control module has an input connected to the signal properties evaluation module 130, discussed in conjunction with Figure 1.

The combiner 516, which receives the signals from each of the fingers of the RAKE receiver, adds each of the multipath signals and provides an output to the other subsystems of the receiver.

In particular, each of the correlators 510 provides a portion of the incoming signal to the combiner 516. In turn, the combiner 516 uses an algorithm to calculate parameter values that aid in the combination of each of the incoming

multipath signals from the correlators 510. These parameter values represent the required time shift, phase shift and amplitude adjustment necessary to properly combine each of the multipath signals. The combiner 516 processes the incoming signals using the parameter calculations and provides a combined signal at the output.

Advantageously, a receiver adopting the principles of the present invention includes the combiner control module 550. The combiner control module 550 provides input to the combiner 516 and each correlator 510 to dynamically adjust the duty cycle of the correlators and the manner of operation of the combiner to reduce power consumption. The combiner control module 550 evaluates various characteristics of the incoming signal and, based on the evaluation, provides appropriate input to the combiner 516 and the correlators 510. The combiner control module 550 obtains information regarding the incoming signal from the signal properties evaluation module 130. In particular, the signal properties evaluation module 130 provides information regarding the signal dynamics, the signal to noise ratio, the signal interference level and the signal power level to the combiner control module 550. Using this information, the combiner control module 550 adjusts the duty cycle of the correlators 510 and the manner of operation of the combiner 516 to reduce power consumption.

With regard to the correlators 510, the combiner control module 550 alters the duty cycle of each correlator based on the incoming signal. For example, if the incoming signal is generally weak and contains a number of multipath components, then the combiner control module 550 enables the maximum number of correlators 510, thereby capturing the weak signal. Alternatively, if the signal properties evaluation module 130 indicates that the signal is generally strong and comprises relatively few (one or two) multipath components, then the control module 550 instructs a number of the correlators 510 to suspend operation. Suspending operation of a number of the correlators 510 reduces the power consumption of the receiver, which extends battery life. Suspending operation of a number of correlators 510 reduces the input to the combiner 516, which consequently reduces the processing burden on the combiner 516. This further reduces the power consumption of the receiver.

The combiner control module 550 also instructs the combiner 516 to dynamically change the algorithms used for parameter estimation. In particular, mobile stations (i.e., a cellular telephone) may operate while stationary or while moving, such as during automobile travel. For a receiver, and in particular the combiner 516, a significant amount of processing (and therefore power) is required to estimate the parameters used to calculate time shift 512, phase shift 520 and amplitude adjustment 530 of each component of the incoming signal before summing with the summer 540 each adjusted signal component. Precise calculation of these parameters is vital during periods when the incoming signal includes significant multipath components, such as for example when the mobile station is moving or when reflecting objects such as building, are intermediate the mobile station and the base station. However, such complex calculations needlessly consume power during periods when the incoming signal does not include a plurality of significant multipath components, such as for example when the mobile station is generally stationary or when it possesses an obstruction free signal path to the base station. Instead of performing complex calculations, the parameters used to determine time shift, phase shift and amplitude adjustment are arrived at using calculations which consume less power or by fixing the

parameter values for certain signal conditions. Thus, the power consumption may be reduced without compromising audio quality or communication link stability.

Figure 7 illustrates an enhanced frequency estimator to provide adaptive frequency estimation (phase reconstruction) such as in the phase/frequency estimator 126 of Figure 1. As seen in Figure 7, there is demodulator 710 provided for a pilot signal and demodulator 712 provided for a desired signal. A phase reconstruction block 714 provides phase estimation for the desired signal. Accordingly, an output of the phase reconstruction block 714 provides an input to the desired signal demodulator 712. The incoming signal (after digital conversion in the present embodiment), provides an input to both the pilot demodulator 710 and the desired signal demodulator 712. The phase reconstruction module 714 receives input from the pilot demodulator 710 and from the signal properties module 130 (see Figure 1). More specifically, the signal properties module 130 provides signals to a dynamic phase reconstruction control module 716 which forms part of the phase reconstruction module 714. The dynamic phase reconstruction control module 716 reacts to information from the signal properties module 130 and from the pilot demodulator 710 to dynamically control the phase reconstruction module 714 to accommodate changing the signal conditions. More specifically, the phase reconstruction module operations can be adaptively controlled to change operations based on the particular signal properties at the time.

As known in the art, a phase reconstruction scheme can be very important because a small error in the estimated phase can result in a large loss for the desired signal. Typically, existing systems utilize the pilot signal which is transmitted at a higher power without full spreading codes so that it is much easier to demodulate. Accordingly, the demodulation allows determination of the phase of the incoming signal. Because the pilot signal and the desired signal are transmitted together, they experience similar or identical paths and interference to the receiver. During periods of high signal dynamics and multi-path components, frequency estimation becomes an important function of the system in order to avoid significant signal losses.

In the present invention, the frequency estimation algorithm, precision, or active periods may be controlled. More specifically, any one or more of the following parameters could be included in selecting two or more algorithms which can be selected based upon the pilot demodulation information or the pilot demodulation together with the signal properties module information. The processing rate may be increased or decreased. Such increase or decrease may be based on power level rather than tracking performance. The phase reconstruction filter 714 may actually be deactivated and activated only a few to several times a second during periods of high signal strength and low signal dynamics and fading. However, during high signal dynamics, where the signal may have multi-path components and the phase is changing rapidly, the filter may run constantly. In addition or alternatively, the precision of the phase reconstruction filter 714 can be modified. For instance, the precision can be changed from 16-bit to 8-bit in one embodiment. In addition or in combination with the other elements, the actual filter type could be changed. For instance, a FIR filter, IIR filter, sliding window filter, or other type of filter could be selected based upon the signal characteristics.

Finally, as shown in Figure 7, the signal properties module 130 could play a significant role in the phase reconstruction decisions. Conventional designs typically involve using the pilot signal to determine frequency estimation. The pilot is easy to demodulate because of its high power and lack of full spreading codes. In spread spectrum systems,

each base station may have many desired signals, each with its own spreading code transmitted in a particular direction from the base station. Typical base stations in spread spectrum systems may have three different directional sections, each which can have 10 to 20 signals with spreading codes (such as Walsh codes) for each signal. Accordingly, the signal from the base station includes a pilot plus several desired signals using several corresponding spreading codes. Typically, each mobile site demodulates the data resulting only from its own spreading code. However, because there are many other coded signals in the same collective signal, the present embodiment also involves utilizing the other spread spectrum signals not intended for the particular receiver in determining the phase reconstruction. In other words, the demodulated desired signal for other users can be used for tracking the phase, and, the tracking can be improved. Of course, the additional demodulation requires additional power; however, in periods of high signal dynamics, such increase in processing may be required in order to maintain a signal for the particular user in question.

In summary, in accordance with this embodiment of the present invention, several different features can come into play in impacting the phase reconstruction (frequency estimation) operations of the receiver.

GSM Demodulator Having Reduced Power Consumption Design

In yet another embodiment, power saving features are integrated with a receiver operating in accordance with Global System for Mobile Communications (GSM).

Figure 6 illustrates a typical Global System for Mobile Communication (GSM) demodulator. Input lines carrying baseband I (in-phase) and Q (quadrature-phase) data connect to an automatic gain control module 610 and a signal level estimator 612. The output of the signal level estimator 612 connects to the AGC module 610.

The output of the AGC module 610 connects to a cross-correlator 614. The cross-correlator's output connects to each of a matched filter 616, a matched filter extractor 618, and a timing recovery unit 620. The output of the matched filter extractor 618 feeds directly into the matched filter 616. The output of the matched filter 616 and the timing recovery unit 620 both connect to a Maximum Likelihood Sequence Estimation (MLSE) detector 622.

The MLSE detector 622 couples to the input of a decryption unit 624 and the output of the decryption unit feeds into a deceiver 626. The deceiver 626 outputs data to a convolutional decoder 630. The convolutional decoder 630 in turn connects to a block decoder 632. The block decoder 632 provides output on a data out line.

In operation, the automatic gain control module 610 adjusts the input signal level of the baseband I and Q data (hereinafter signal) for optimal performance during the subsequent demodulation operations as well understood in the art. The incoming signal also enters a signal level estimator 612 that estimates the power level of the incoming signal. Estimating the signal power level serves two purposes; first, a GSM communication system adapts its performance based on the strength of the received signal at each of the mobile stations; and second, the receiver adjusts the gain of the input signal for subsequent demodulation processes. Accordingly, the demodulator provides the output of the signal level estimator 612 to the AGC module 610 so that the gain of signal may be adjusted appropriately.

The cross-correlator 614 compares the received data to a known training sequence or a training sequence included mid-sample in the received data burst. The cross-correlator locates the beginning of each burst of data using the known 26 symbols located at the center of each burst. As known in the art, bursts are sent in a generally .5 millisecond

time frame followed by 4.5 millisecond pause. The cross-correlator, having located or correlated the known 26 symbols is able to locate the beginning of the data transmission.

Next, the signal undergoes filtering and timing recovery. The matched filter extractor 618 models an ideal matched filter to reverse the effects of the transmission channel and any inter-symbol interference introduced by the pulse shape. The timing recovery unit 620 determines the proper timing of the incoming signal to locate the center of the burst which in-turn allows the receiver to correctly separate and demodulate the individual symbols.

The next phase of the demodulation process comprises MLSE detection. The MLSE detector 622 performs a sophisticated detection algorithm that declares each received symbol to be a 1 or 0 and provides a measure of the certainty of each binary decision. As known in the art, the algorithms of the MLSE detector 622 employ a dynamic programming model to simultaneously demodulate an entire half-burst (typically 58 bits) of data. While certain advantages exist in performing demodulation over the half-burst instead on a symbol-by-symbol bases, half-burst demodulation consumes a significant amount of power during operation.

After MLSE detection, the signal enters a decryption unit 624 to reverse the anti-eavesdropping measures undertaken by the transmitter. Next, the signal enters the deleaver 626, wherein the transmitted bits are dispersed over several time division multiple access (TDMA) bursts to provide robustness in the presence of fading. The deleaver 626 rearranges the received bits into message blocks i.e. into the original order existing prior to transmission.

The output of the deleaver 626 progresses to the input of the convolutional decoder 630. The convolutional decoder 630 performs convolutional decoding on the received data. Convolutional coding and decoding provides means to detect and correct data errors introduced during transmission. In particular, convolutional coding adds coding to the data so that the convolutional decoder may accurately reconstruct the transmitted data, even if some of the data bits become corrupted during transmission.

After convolutional decoding, the signal enters the block decoder 632 to undergo reverse block coding. Block coding provides redundancy, typically parity bits. These parity bits are typically often transmitted at the end of a sequence of data bits so that upon receipt by the receiver, the block decoder 632 may perform reverse block coding to determine if errors exist in the data stream. After undergoing block decoding, the signal exits the block decoder 632 for further processing in other parts of the receiver, such as a vocoder (not shown).

In one embodiment of the present invention, the receiver comprises a digital signal processor (DSP) coded implementation of a GSM receiver. The inventors recognize that the most complex and power consuming operation is typically the MLSE detection algorithm of the MLSE detector 622. For example, in some DSP based implementations, the MLSE detection may comprise up to 50% of the complexity in relation to total DSP operations. While the advantages of the MLSE detector are worthy of its power needs during periods of poor signal quality, the MLSE detector needlessly consumes power when the signal is robust.

Another very complex and power consuming component is the cross-correlator 614 because it operates over a broad range of delays to correctly locate the center of the data burst. Cross-correlation in DSP based implementations may comprise up to 30% of the total DSP operations.

In one embodiment, a GSM receiver is configured to eliminate a substantial portion of the computational requirements of the receiver by monitoring the timing recovery unit 620 for rapid movement from center on a burst-by-burst basis. In such an embodiment, the receiver would also include a cross-correlator controller 616. The cross-correlator controller 616 connects to the cross-correlator and the timing recovery unit. The cross-correlator controller 616 obtains data from the timing recovery unit 620 and depending on the timing of the incoming signal, changes the operation of the cross-correlator accordingly. In particular, if the incoming signal does not demonstrate rapid movement from burst center then the cross-correlator controller 616 instructs the cross-correlator 614 to operate over a more narrow range of delays. For example, in normal operation the cross-correlator 614 may operate over ± 5 data symbols. Under ideal situations, such as when the burst center is generally stable, performing cross-correlation over ± 2 symbols may be adequate. In short, when assuming the data transmission to be generally stable, the cross-correlator can anticipate little change in burst center and reduce computational complexity such as, for example, evaluating fewer symbols. Reducing the computational complexity and duration of the cross-correlator 614 reduces the power consumption of the receiver which, in turn, extends battery life. If the timing recovery unit 620 detects rapid movement from burst center, then the cross-correlator controller 616 instructs the cross-correlator 614 to resume operation over a broader range of delays. In this fashion, the cross-correlator controller 616 adjusts the operation of the cross-correlator 614 to save power during periods when the signal is stable without degrading signal quality.

In another embodiment, the receiver includes a MLSE controller 621 connected to the MLSE detector 622, the matched filter 617, and the output of the signal level estimator 612. The MLSE controller receives input from the matched filter 616 and the signal level estimator 612. The MLSE controller 621 monitors both the signal level of an incoming transmission and the response to the matched filter 617. If the incoming signal level is high and the response to the match filter 617 indicates that the signal is arriving over a generally clear channel, then the receiver suspends operation of the complicated MLSE detector 622, and instead implements a simple bit-by-bit Minimum Shift Keying (MSK) demodulator. MSK demodulators are known by those of skill in the art, and require a trivial amount of computational resources, and thus battery power, in relation to the MLSE algorithms of the MLSE detector 622 due to their operation on a bit-by-bit basis instead of the typical 58 bit delay of the MLSE detector 622.

A receiver adopting MSK demodulation over MLSE algorithms consumes less power than a receiver utilizing only MLSE detection algorithms. Thus, if the signal is robust, the power intensive MLSE detector operation may be suspended and replaced with bit-by-bit MSK demodulation. Alternatively, if the signal changes causing the response to the matched filter 617 to not resemble a impulse and if the signal level decreases, then the MLSE controller 621 suspends operation of the bit-by-bit MSK demodulator and resumes operation of the MLSE algorithms. In this fashion, the MLSE controller 621 reduces power consumption of the receiver without sacrificing audio quality. As explained in the embodiment above, the signal level estimator and the match filter are used to determine the signal quality. Other quality measurements such as automatic gain control could be used to indicate the receiver algorithm which will be implemented for the remainder of the receiver.

Although the foregoing description of the preferred embodiment of the present invention has shown, described and pointed out the fundamental novel features of the invention, it will be understood that various omissions, substitutions and changes in form of the detail of the apparatus as illustrated as well as the uses thereof, may be made by those skilled in the art without departing from the spirit from the present invention. Consequently, the scope of the invention should not be limited to the foregoing discussion, but should be defined by the appended claims.

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WHAT IS CLAIMED IS:

1. A power utilization control system for a wireless communication device, comprising:
a signal properties evaluation module, said module operative to evaluate the characteristics of a received signal, said module configured to provide an indication of said characteristics; and
5 at least one receiver component for said wireless communication device, said receiver component having at least two modes of operation, said receiver component responsive to said signal properties evaluation module to operate in at least one of said at least two modes of operation, based upon the said characteristics.
2. The power utilization control system of Claim 1, wherein signal properties evaluation module is implemented using a digital signal processor.
- 10 3. The power utilization control system of Claim 1, wherein said signal properties evaluation module is configured to evaluate any of signal dynamics, signal noise levels, or signal strength.
4. The power utilization control system of Claim 1, wherein said wireless communications receiver operates in accordance with code division multiple access.
5. The power utilization control system of Claim 1, wherein said at least one receiver component
15 comprises at least one analog to digital converter configured to convert said received signal in an analog format to a received signal in a digital format, wherein said first mode comprises operation at a first precision and said second mode comprises operation at a second precision, said power utilization control system further comprising:
an analog to digital converter control module responsive to said signal properties evaluation module to
select the precision of said at least on analog to digital converter based upon said indication of signal
20 characteristics.
6. The power utilization control system of Claim 5, wherein said analog to digital converter control module is configured to select a lower bit precision for said at least one analog to digital converter when the signal is of generally high quality.
7. The power utilization control system of Claim 1, wherein said at least one receiver component further
25 comprises a plurality of despread modules, said despread modules responsive to said indication of said characteristics from said signal properties evaluation module to adjust operation based upon said indication of signal characteristics.
8. The power utilization control system of Claim 1, wherein said at least one receiver component comprises a timing estimator, said timing estimator responsive to said indication of said characteristics from said signal properties evaluation module to alter timing estimation operation based upon said indication of signal characteristics.
- 30 9. The power utilization control system of Claim 8, wherein said at least one receiver component further comprises a plurality of despread modules, said despread modules responsive to said indication of said characteristics from said signal properties evaluation module to adjust operation based upon said indication of signal characteristics.
10. The power utilization control system of Claim 9, wherein said despread modules respond to said indication of said signal characteristics via a control unit to adapt one or more of the operation duty cycle or tap spacing in
35 response to said indication of signal characteristics.

11. The power utilization control system of Claim 8, wherein said timing estimator responds to said indication of said signal characteristics via a timing control unit to modify one or more of the timing estimator type, operation duty cycle, and bandwidth.
12. The power utilization control system of Claim 8, wherein said timing estimator comprises a delay-lock-
5 loop.
13. The power utilization control system of Claim 1, wherein said at least one receiver component comprises at least one equalizer, said at least one equalizer responsive to said indication of signal characteristics from said signal properties evaluation module to change its operation based upon said indication of signal characteristics.
14. The power utilization control system of Claim 13, wherein said equalizer alters one or more of its duty
10 cycle or complexity of operation based upon said indication of signal quality.
15. The power utilization control system of Claim 1, wherein said at least one receiver component comprises at least one correlator, said correlator responsive to said indication of signal characteristics to operate in either said first or said second mode.
16. The power utilization control system of Claim 15, wherein said first mode comprises operation at a
15 first precision and said second mode comprises operation at a second precision.
17. The power utilization control system of Claim 16, wherein said first mode of operation further includes a first duty cycle for said correlator and said second mode of operation comprises a second duty cycle for said at least one correlator.
18. The power utilization control module of Claim 1, wherein said signal properties evaluation module
20 provides said indication of said characteristics via a control module.
19. The power utilization control system of Claim 18, wherein said at least one receiver component comprises a plurality of correlators, said control module suspending operation of one or more of said plurality of correlators during periods when the signal is of relatively good quality.
20. The power utilization control system of Claim 1, wherein said at least one receiver component
25 comprises a signal combiner, said signal combiner responsive to said indication of signal characteristics from said signal properties evaluation module to alter operation of said combiner based upon said indication of signal characteristics.
21. The power utilization control system of Claim 20, wherein said at least two modes comprise a first mode wherein said combiner operates in accordance with a first processing algorithm and a second mode wherein said signal combiner operates in accordance with a second algorithm.
- 30 22. The power utilization control system of Claim 21, wherein said first algorithm comprises a more complex algorithm than said second algorithm.
23. The power utilization control system of Claim 1, wherein said at least one receiver component comprises a frequency estimation module, wherein said at least two modes comprise at least first and second modes selected in response to said indication of said signal characteristics from said signal properties evaluation module.

24. The power utilization control system of Claim 23, wherein said at least two modes comprises at least two algorithms, said at least two algorithms having a difference in one or more of the processing precision, filter type, processing rate, or duty cycle.

25. The power utilization control system of Claim 23, wherein said frequency estimation module responds to a demodulated pilot signal and to demodulated desired signals from users other than the intended receiver.

26. A method of reducing power consumption in a wireless communication receiver having a plurality of receiver components comprising:

receiving a signal;

monitoring the characteristics of the incoming signal;

evaluating the characteristics of the incoming signal; and

altering the operation of at least one of said receiver components based upon the evaluated quality of the incoming signal.

27. The method of reducing power consumption of Claim 26, wherein said at least one of said receiver components comprises an analog to digital converter.

28. The method of Claim 27, wherein altering the operation of said analog to digital converter comprises altering the precision of the analog to digital converter.

29. The method of Claim 28, wherein altering the precision of the analog to digital converter comprises altering the precision between 5 bits and 2 or 3 bits.

30. The method of Claim 27, wherein monitoring the characteristics of the incoming signal comprises monitoring any of signal dynamics, signal noise, signal level, bit error rate, or field error rate.

31. The method of Claim 30, wherein said method is implemented in a communication receiver operating in accordance with code division multiple access.

32. The method of Claim 27, wherein evaluating the quality of said incoming signal comprises determining the proper precision setting for said one or more analog to digital converters.

33. The method of Claim 26, wherein said step of altering the operation of at least one of said receiver components comprises adjusting the operation of signal timing estimator.

34. The method of Claim 33, wherein said signal timing estimator comprises at least one delay lock loop.

35. The method of Claim 33, wherein said step of adjusting operation comprises reducing the duty cycle of said timing estimator.

36. The method of Claim 35, wherein said step of monitoring the signal comprises monitoring any of signal dynamics, signal noise, and signal level.

37. The method of Claim 33, wherein step of adjusting operation comprises adjusting the filter properties of a timing estimator.

38. The method of Claim 26, wherein said step of evaluating comprises evaluating the difference between the output of two correlators.

39. The method of Claim 26, wherein said step of altering the operation of at least one of said receiver components comprise altering the operation of an equalizer for an incoming signal, said method further comprising the steps of evaluating information regarding the characteristics of an incoming signal; and modifying the complexity of equalizer algorithms for said equalizer based upon said evaluation.

5 40. The method of Claim 26, wherein said step of altering the operation of at least one of said receiver components comprises altering the operation of at least one correlator based upon the evaluation of the incoming signal.

41. The method of Claim 40, wherein said step of altering the operation of at least one correlator comprises modifying the symbol frequency of operation of the correlator.

10 42. The method of Claim 26, wherein said step of altering the operation of at least one of said receiver components comprises altering the operation of a signal combiner in response to said step of evaluating the quality of the incoming signal.

43. The method of Claim 42, wherein said step of altering the operation of a signal combiner comprises selecting one of at least two algorithms operable with the said combiner.

15 44. The method of Claim 26, wherein said step of altering the operation of at least one of said receiver components comprises altering the operation of a frequency estimator in response to said step of evaluating the quality of the incoming signal.

45. The method of Claim 44, wherein said step of altering the operation of a frequency estimator comprises selecting an algorithm from at least two algorithms operable for said frequency estimator.

20 46. The method of Claim 44, wherein said step of altering the operation of said frequency estimator comprises selecting a precision for said frequency estimator.

47. The method of Claim 44, wherein said step of altering the operation of a frequency estimator comprises controlling active periods for said frequency estimator.

25 48. An adaptive signal synchronization apparatus for a wireless receiver comprising:
a timing estimator;
a signal properties evaluation module responsive to signal characteristics to evaluate an incoming signal; and
a timing controller responsive to said signal properties evaluation module to control the operation of said timing estimator.

30 49. The adaptive signal synchronization apparatus of Claim 48, wherein said timing estimator includes at least one delay lock loop.

50. The adaptive signal synchronization apparatus of Claim 48, wherein said timing controller is configured to adapt the percentage of time that said timing estimator operates.

51. The adaptive signal synchronization apparatus of Claim 48, wherein said timing controller is configured to control tap spacing of said timing estimator.

52. The adaptive signal synchronization apparatus of Claim 48, wherein one or more of said timing estimator, said timing controller and said evaluation module are embodied with a digital signal processor.

53. The adaptive signal synchronization apparatus of Claim 48, further comprising a plurality of despread modules, said despread modules responsive to an indication of signal characteristics from said signal properties evaluation module to adjust operation of despread modules.

54. An adaptive equalizer system for a wireless receiver comprising:
an equalizer operable in at least two modes to perform equalization on an incoming signal;
a signal properties evaluation module responsive to signal characteristics to evaluate an incoming signal; and

an equalizer controller responsive to said signal properties evaluation module to select between said at least first and second modes.

55. The adaptive equalizer system of Claim 54, wherein said equalizer controller is embodied in a digital signal processor.

56. The adaptive equalizer system of Claim 54, wherein said signal properties evaluation module is embodied in a digital signal processor.

57. The adaptive equalizer system of Claim 54, wherein said signal properties evaluation module receives a plurality of characteristics of an incoming signal and responds to such characteristics to develop equalizer operating parameters.

58. The adaptive equalizer system of Claim 54, wherein said at least first and second modes of operation comprise a first mode in which said equalizer operates in accordance with a first algorithm and a second mode wherein said equalizer operates in accordance with a second algorithm which is different from said first algorithm.

59. The adaptive equalizer system of Claim 54, wherein said receiver comprises a wireless communication receiver in a wireless communication system.

60. The adaptive equalizer system of Claim 54, wherein said equalizer is configured to compensate for time delays introduced in a signal transmitted over a wireless medium.

61. A method for adaptive operation of an equalizer in a receiver comprising:
receiving, equalizing and demodulating an incoming signal;
evaluating the quality of the incoming signal; and
adapting the operation of an equalizer based on said step of evaluating.

62. The method of Claim 61, wherein said adapting the operation of an equalizer comprises shutting off said equalizer when said evaluating indicates the signal is of generally high quality.

63. The method of Claim 61, wherein said adapting the operation of an equalizer comprises reducing the computational complexity of said equalizer when said evaluating indicates the incoming signal is of generally high quality.

64. The method of Claim 61, wherein evaluating comprises evaluating any of signal dynamics, signal noise, signal level, bit error rate, or frame error rate.

65. The method of Claim 64, wherein evaluating comprises determining the rate of change over time of one or more of the signal dynamics, signal noise, signal level, bit error rate or frame error rate.

66. An adaptive combiner for a receiver comprising:

at least two correlators configured to receive an incoming signal;

a combiner coupled to said at least two correlators;

a signal properties evaluation module responsive to characteristics of a received signal to provide an indication of the properties of an incoming signal; and

a combiner control module coupled to said combiner and responsive to said indication of signal characteristics from said signal properties evaluation module to alter operation of said combiner based upon said indication of said signal characteristics.

67. The apparatus of Claim 66, wherein said combiner control module is further coupled to at least one of said at least two combiners, said combiner control module configured to provide a control signal to at least one of said at least two combiners to alter the operation of at least one of said at least two combiners.

68. The apparatus of Claim 67, wherein at least one of said correlator, said combiner, said signal properties evaluation module and said combiner control module is embodied using a digital signal processor.

69. The apparatus of Claim 67, wherein said combiner comprises part of a wireless communication receiver.

70. A method of adaptive control in a receiver comprising:

receiving an incoming radio signal;

correlating at least portions of the incoming signal;

combining said portions of the incoming signal

evaluating the quality of the incoming signal; and

controlling said combining step based on the quality of the incoming signal.

71. The method of Claim 70, wherein said step of combining may proceed in accordance with a first or a second mode of operation, said first and second mode operating in accordance with different algorithms for said combining step, said controlling comprises changing said mode.

72. The method of Claim 70, wherein said algorithms differ in the manner of parameter estimation used in said step of combining.

73. The method of Claim 70, wherein said evaluating comprises evaluating one or more of the signal dynamics, signal noise, signal level, bit error ratio, and frame error ratio.

74. A method for reducing power consumption in a receiver operating in accordance with the principles of Global System for Mobile Communications comprising:

receiving a radio signal;

evaluating signal dynamics of said radio signal; and,

altering a range of delays in a correlator based on said signal dynamics.

75. The method of Claim 74, wherein said step of evaluating comprises monitoring in a timing unit the rate of signal timing change over time.

76. The method of Claim 75, wherein said step of altering a range of delays comprises reducing the range of delays when said signal is determined to be generally stable based on said signal dynamics.

5 77. The method of Claim 76, wherein generally stable comprises a low rate of change over time.

78. The method of Claim 77, wherein a generally stable signal comprises a signal wherein the signal does not demonstrate rapid timing drift from burst center.

79. The method of Claim 77, wherein reducing the range of delays comprises performing cross-correlation every ± 2 data symbols.

10 80. The method of Claim 74, wherein said step of evaluating comprises monitoring the center of a burst from burst to burst in the received radio signal.

81. The method of Claim 74, wherein said step of altering a range of delays comprises increasing the range of delays and said signal dynamics indicate that said radio signal is generally unstable based on high signal dynamics.

15 82. An adaptive correlator for a communications receiver configured to receive an incoming signal comprising:

a correlation unit configured to compare said incoming signal to a known timing sequence.

a timing recovery unit connected to said correlation unit, said timing recovery unit configured to evaluate the timing of said incoming signal;

20 a correlator controller connected to both of said timing recovery unit and said correlation unit, said correlation controller configured to adapt the operation of said correlation unit based on said evaluation by said timing recovery unit.

83. The adaptive correlator of Claim 82, wherein said correlator controller is configured to adapt the operation of said correlation unit to reduce the number of symbols over which the correlation unit operates.

25 84. The adaptive correlator of Claim 82, wherein said timing recovery unit is configured to determine the change in timing of said incoming signal over time.

85. The adaptive correlator of Claim 82, wherein said correlator unit is configured to perform a cross-correlation between the received signal and a known training sequence.

86. The adaptive correlator of Claim 82, wherein said communications receiver operates in accordance with the principles of a Global System For Mobile Communications.

30 87. A method of adaptive control in a receiver utilizing MLSE algorithms comprising:
receiving signal;

monitoring the level of said signal;

monitoring the response of said incoming signal to a filter; and

35 suspending operation of said MLSE algorithms when said signal level is high and said response to said filter indicates a generally clear channel.

88. The method of Claim 87, wherein a high signal level comprises a signal having level generally near the maximum signal level.

89. The method of Claim 87, wherein monitoring the level comprises monitoring the output of a signal level estimator.

5 90. The method of Claim 87, wherein monitoring the response comprises monitoring the response of said incoming signal to a matched filter.

91. The method of Claim 87, wherein a generally clear channel comprises a response to said filter generally resembling an impulse.

10 92. The method of Claim 87, wherein suspending said MLSE algorithm comprises replacing said MLSE algorithm with a MSK demodulator.

93. The method of Claim 92, wherein said MSK demodulator comprises a bit-by-bit MSK demodulator.

94. An adaptive MLSE detector comprising:

a signal level estimator responsive to an incoming signal to determine the signal level of said incoming signal;

15 a filter configured to filter said incoming signal;

a MLSE detector configured to obtain input from said filter, said MLSE detector configured to compute signal probability; and

20 a MLSE controller coupled to said signal level estimator, said filter and said MLSE detector, said MLSE controller configured to evaluate output from said signal level estimator and said filter and, based on said evaluation, control the operation of said MLSE detector.

95. The adaptive detector of Claim 94, wherein said filter comprises a matched filter.

96. The adaptive detector of Claim 94, wherein said MLSE controller is configured to suspend operation of said MLSE algorithms when said signal level estimator indicates said signal is generally high and said response to said signal is generally an impulse.

25 97. The adaptive detector of Claim 96, wherein said MLSE controller is configured such that when said MLSE algorithms are suspended, said MSK demodulation occurs.

98. The adaptive detector of Claim 94, wherein control of the operation comprises reducing the power consumption.

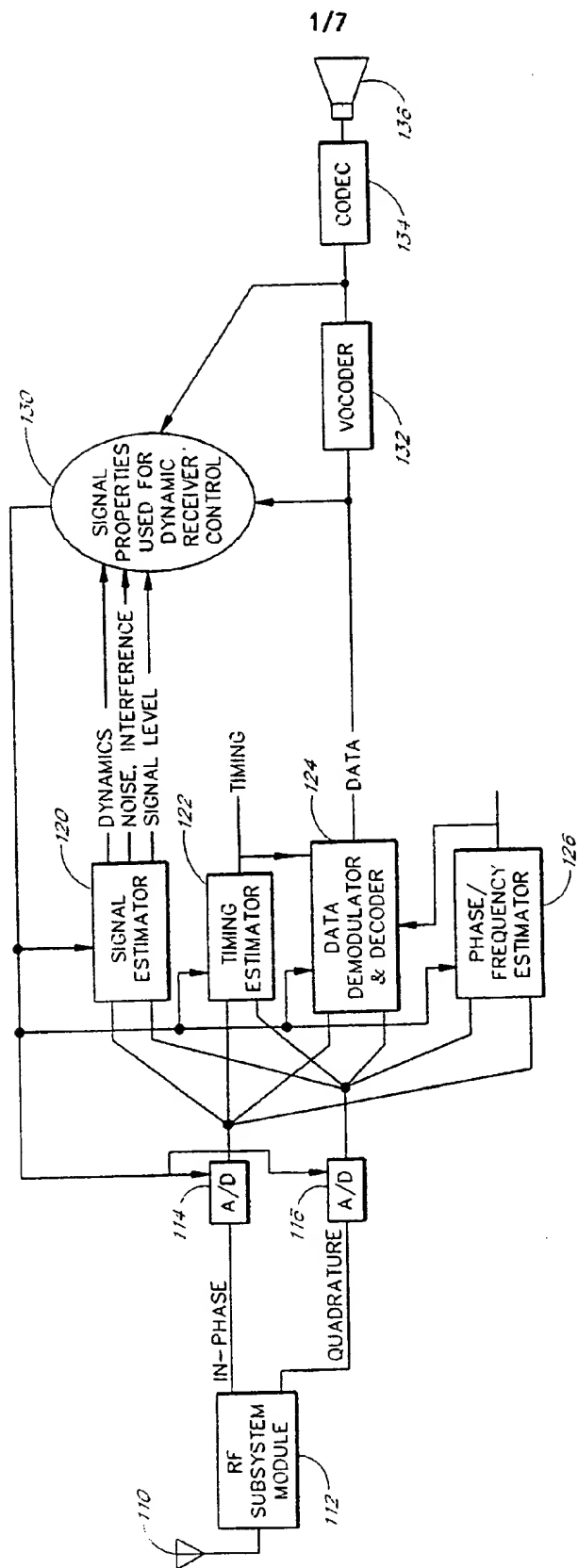


FIG. 1

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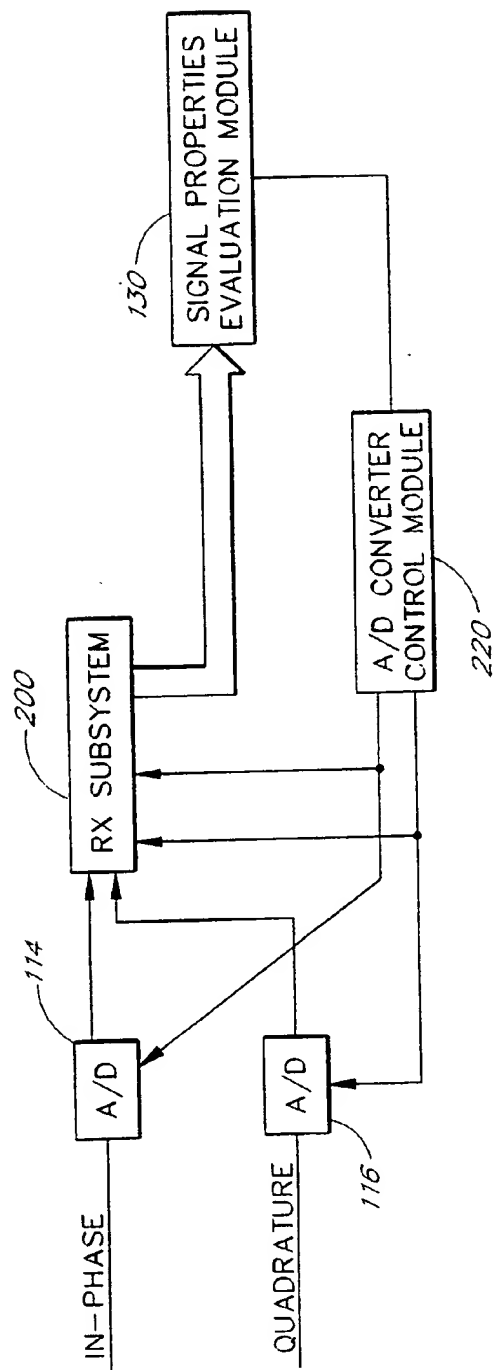


FIG. 2

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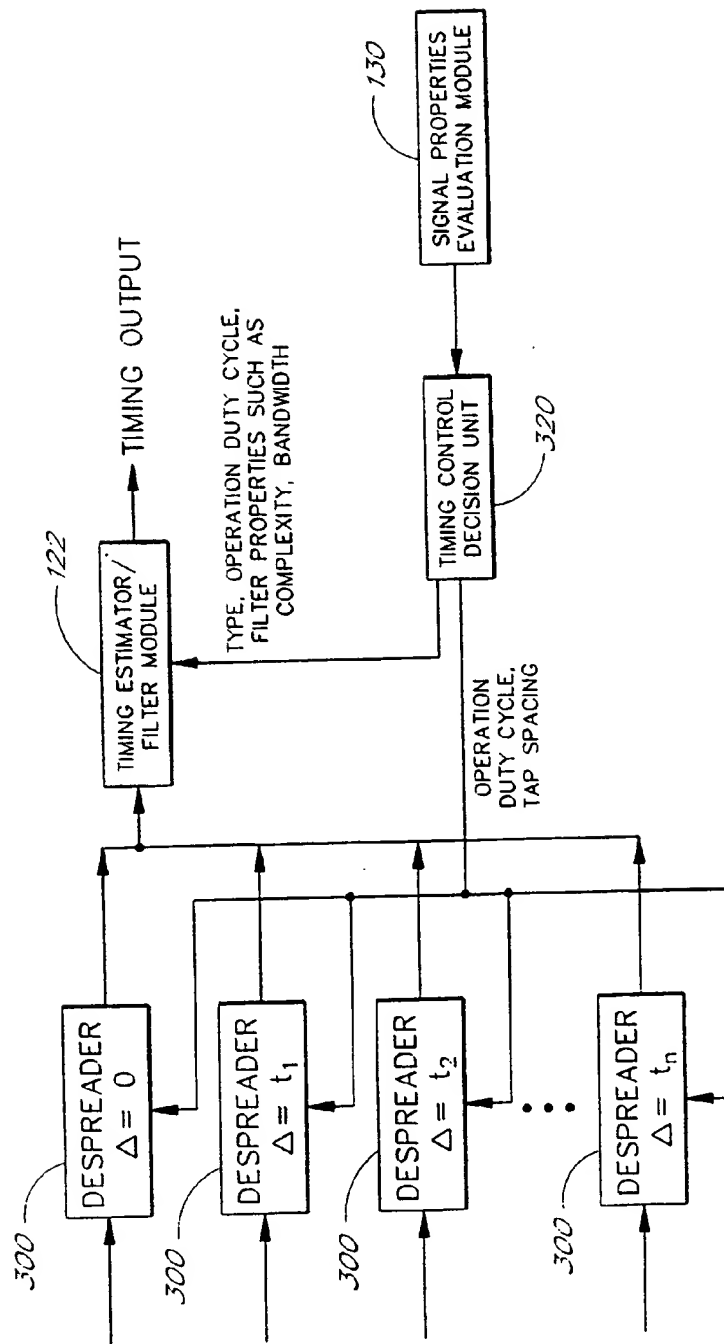


FIG. 3

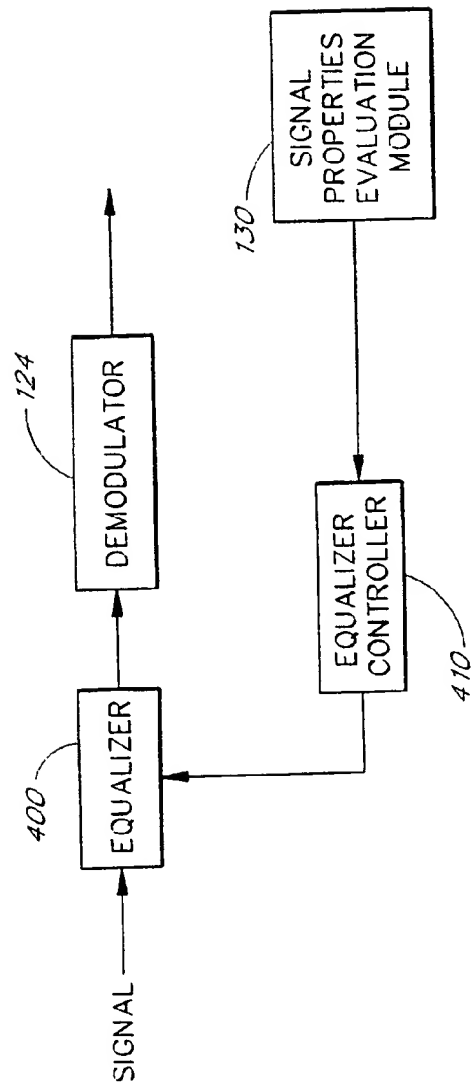


FIG. 4

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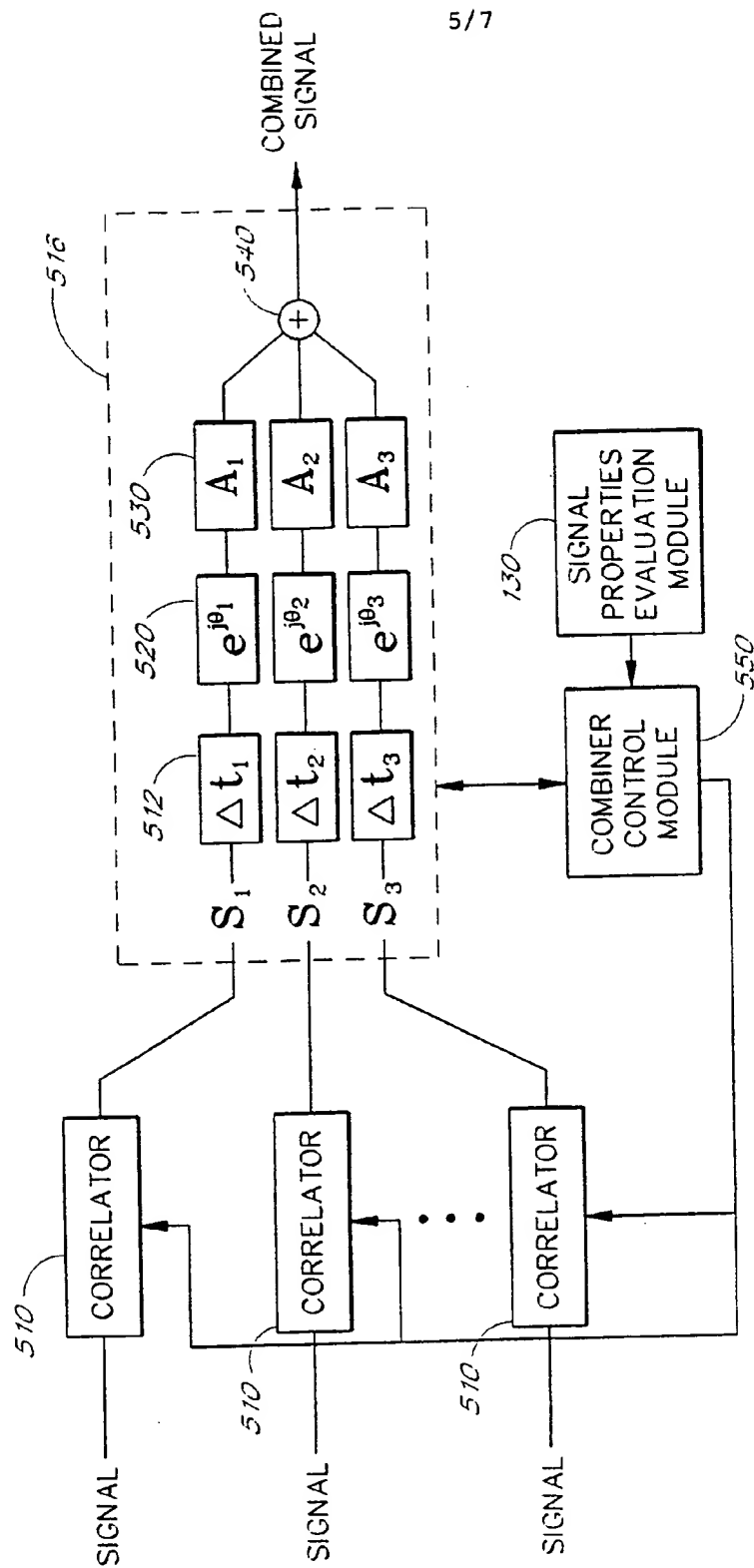


FIG. 5

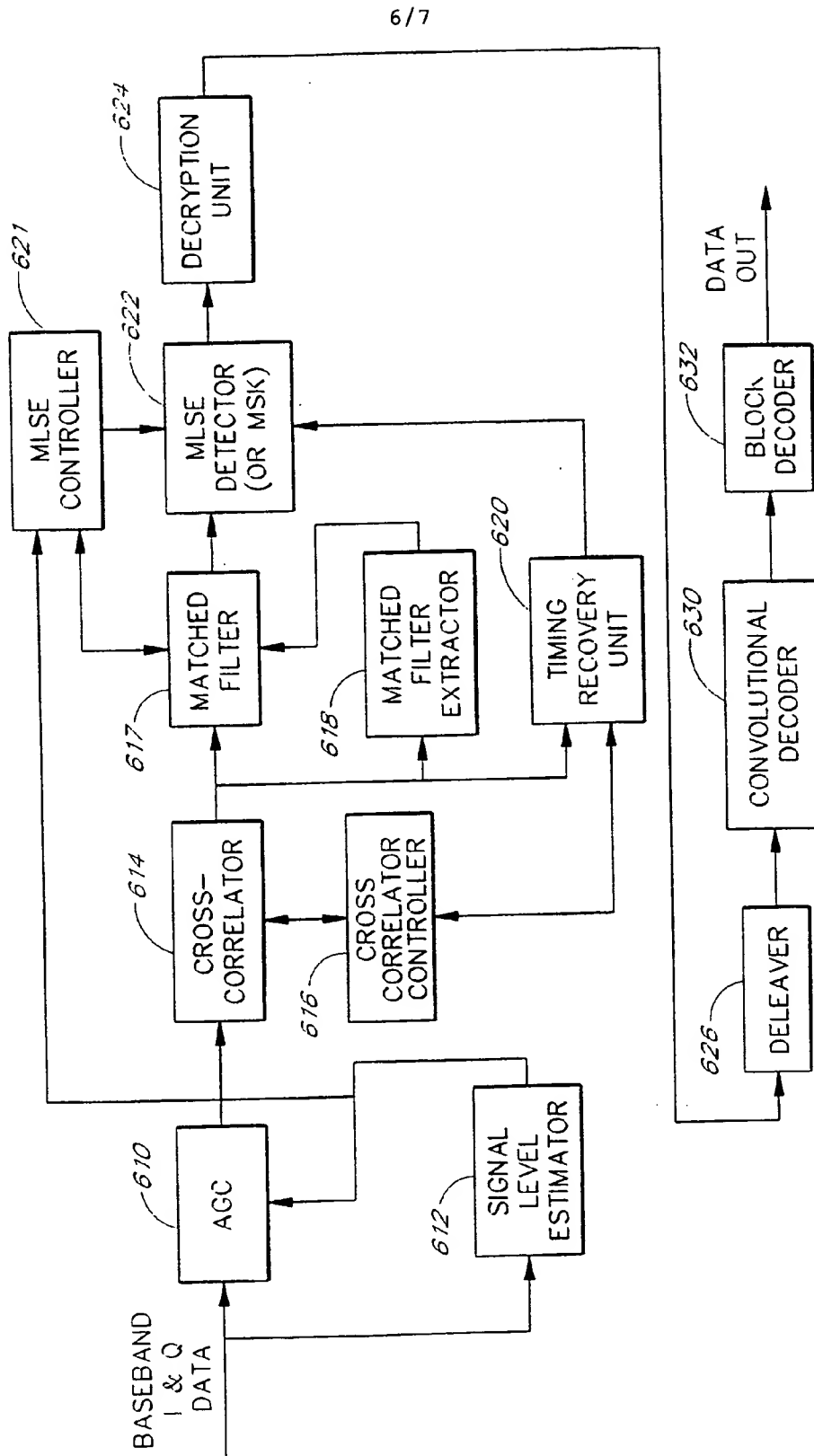


FIG. 6

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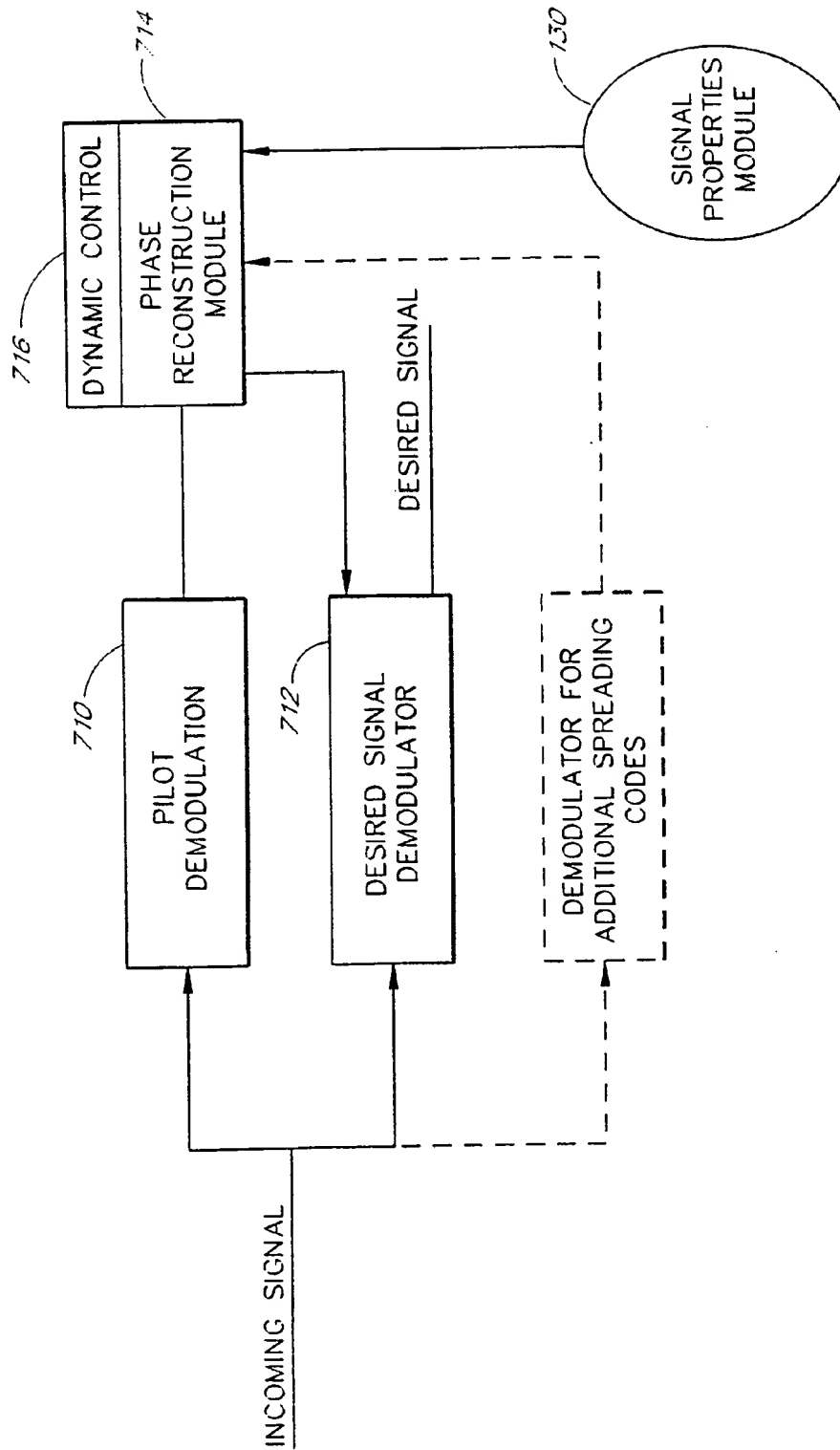


FIG. 7

INTERNATIONAL SEARCH REPORT

International Application No

LT/US 99/22080

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H04B17/00 H04B1/707

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 H04B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 92 13392 A (ERICSSON GE MOBILE COMMUNICAT) 6 August 1992 (1992-08-06) abstract page 2, line 23 -column 3, line 10 ---	1-3,26
X	EP 0 639 901 A (HITACHI LTD ;HITACHI MICROCOMPUTER SYST (JP)) 22 February 1995 (1995-02-22) abstract; figures 6,7,10 column 13, line 57 -column 14, line 52 column 17, line 11 - line 42 claims 14,15,17-19 --- -/--	1-3,26

☒ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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Date of the actual completion of the international search

19 January 2000

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INTERNATIONAL SEARCH REPORT

International Application No

PCT/US 99/22080

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication where appropriate, of the relevant passages	Relevant to claim No.
X	<p>PATENT ABSTRACTS OF JAPAN vol. 1996, no. 07, 31 July 1996 (1996-07-31) & JP 08 065205 A (MATSUSHITA ELECTRIC IND CO LTD), 8 March 1996 (1996-03-08) abstract -----</p>	1-4,26

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Information on patent family members

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